

# VERSATILITY AND MANUFACTURABILITY CONSIDERATIONS FOR A NEW 3-WATT X-BAND POWER MMIC

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## Abstract

The paper presents a newly developed two-stage power amplifying MMIC capable of delivering 3 Watt at X-band with high efficiency. This MMIC is designed for operation with external matching circuits on separate ceramic substrates. By customizing these circuits, the same MMIC can cover an entire array of different applications. The versatility of this approach is demonstrated by the implementation of this MMIC in four power modules specified for different bandwidths, power levels and bias voltages. The small chip size and the tunability allowed by the external circuits lead to increased manufacturing yields and make possible significant cost reductions.

## Introduction.

The concept of partially matched power-amplifying MMICs [1] was developed as a trade-off between the monolithic and hybrid technologies, leading to low cost, high performance and increased versatility. It consists of including on the GaAs chip the essential elements only: the active devices, the interstage matching network and part of the input circuit. The output impedance transformer and most of the input circuit are realized on separate substrates, and allow some degree of customization for specific implementations. The present paper describes the utilization of a MMIC designed along these lines in applications differing both in frequency range and bias conditions.

## Circuit design.

The MMIC is a two-stage amplifying circuit that delivers 3 W in X-band. The power FET has a 7.2 mm gate periphery (80 fingers 90  $\mu\text{m}$  long) and the driver FET has a 2.76 mm gate periphery (40 fingers 69  $\mu\text{m}$  long).

The full output power capabilities of a FET are realized only as long as the load it sees has a particular impedance (optimal for power). For this purpose, the output circuit transforms the amplifier load into the impedance required by the device. The precision with which this match can be achieved decreases as the frequency range specified becomes wider. The optimum load depends also on the drain bias voltage. The ability to customize the load that the power FET looks into, with no change in the chip layout, makes a whole range of applications available, without unnecessary sacrifices in the output power.

The load of the driver, however, is determined by the MMIC configuration. Versatility requires a broadband match between the input of the power FET and the output of the driver FET, over the maximum range contemplated for different applications. For the same reason, the impedance presented to the driver should be a reasonable compromise between the optimum values for different drain voltages. Both factors imply an unavoidable penalty in the power per gate-length the driver can deliver, so that a generous margin has to be allowed when selecting its size. This translates into a reduction of the power-added-efficiency (since a larger driver will draw a proportionally larger drain current) and the design challenge is to minimize this negative effect.

The interstage circuit includes a number of elements imposed by bias considerations (shunt inductive branches through which gate and drain voltages are applied and a blocking capacitor separating the two DC voltage levels). They were used also for the purpose of impedance transformation, so that the number of additional elements needed could be kept to a minimum. Lossy resonant branches across the input of the power FET were included, to partially offset the variation of gain versus frequency and to reduce the Q.

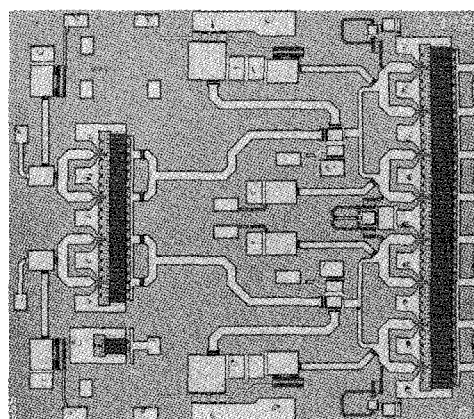


Fig. 1: Microphotograph of the 3W X-band power MMIC

The input circuit of the driver FET was designed for gain flatness, by tailoring the dependence of its reflection coefficient versus frequency so as to compensate the gain-frequency slope. Here too, by keeping the input circuit of the MMIC on a separate substrate, it becomes possible to customize it for applications covering different frequency ranges. The input ports of both FETs are points where the impedance levels reach minimum values. In such points, bondwires (equivalent to series inductors) would introduce an element of variability, undesirable from the viewpoint of manufacturing. The interstage part of the MMIC takes care of this for the input of the final FET, which is the most critical. For the driver FET as well, however, the closest and more critical

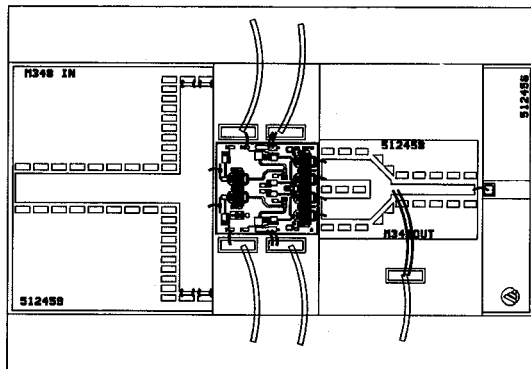


Fig. 2: Layout of the 3W 8.5-10.5 GHz single-ended module

elements of the input circuit (shunt inductors next to the gate and series blocking capacitors) were included on the chip. Together, they bring the low input impedance of the first FET to more manageable values, for which uniformity of the bondwires becomes less significant. Further matching, accomplished by the external circuit, is straightforward and can be obtained with simple configurations.

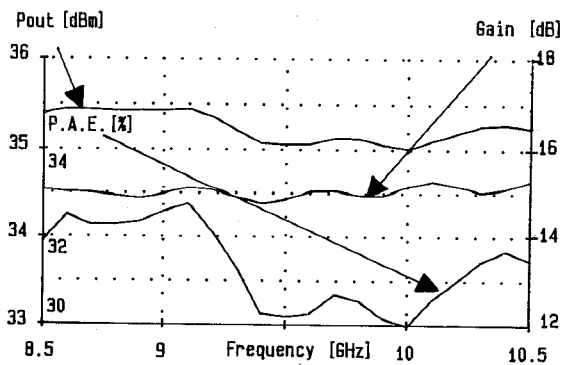


Fig. 3: Performance of the 3W module from Fig. 2

Details regarding the fabrication process and the FET structure have been published previously [2].

The MMIC area is 2.1 mm x 1.85 mm. Its thickness is 0.076 mm. The layout can be seen in Fig. 1.

#### Applications and Performance.

The first application of the MMIC described above was in a single-ended amplifier for the 8.5 - 10.5 GHz band, biased with a drain voltage of +9 V. The layout, presented in Fig. 2, illustrates the partially matched MMIC approach, with the chip inserted between an external input circuit built on an Alumina substrate and an output circuit built on Titanium Oxide. Fig. 3 shows the average data for the prototypes measured. The output power, defined for 2 dB gain compression, exceeds 35 dBm. The associated gain stays close to 15 dB throughout the range. The power added efficiency is better than 30%. The module fits on a carrier that is only 6 mm x 10.5 mm in size.

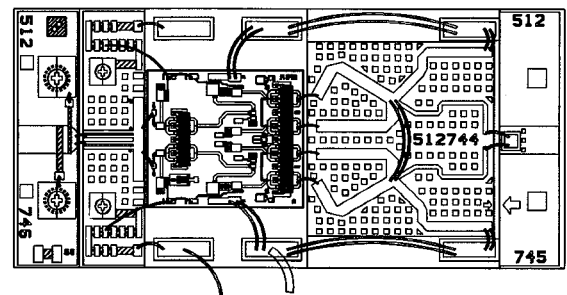


Fig. 4: Layout of the 2W 7-11 GHz module

Another application of the same MMIC was developed for a broader band (7 - 11 GHz) product. The available drain voltage was only +7 V. Full performance (33 dBm) was required between 7.5 and 10.5 GHz, the specification allowing a rolloff up to 30 dBm at the band edges. As Fig. 5 indicates, this target was comfortably reached, with a power-added efficiency exceeding 30% over most of the band and dropping to 25% in the vicinity

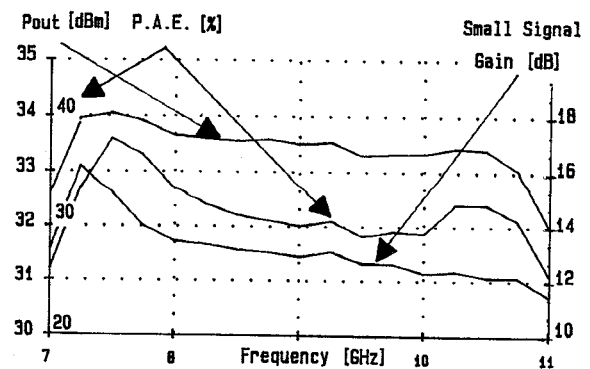


Fig. 5: Performance of the 2W module from Fig. 4

of both ends. The amplifier is designed to operate at saturation, with a fixed input power, so the small signal gain is given only informatively. It varies between 11 and 16 dB, and this figure includes the effect of an adjustable input attenuator, built on the input substrate, which was required because of constraints imposed on the compression level. Since miniaturization was in this case a key consideration, high dielectric constant Titanium Oxide substrates were used for both input and output. As a result, the overall size could be reduced to 3.5 mm x 7.4 mm. The layout of this power module is shown in Fig. 4.

A further application combines two balanced MMICs for an output of 6 W in the frequency range of 8.5 to 10.5 GHz. The drain voltage was +10 V. Fig. 7 shows that the output power measured at 2 dB gain compression exceeded 38 dBm. The associated gain, varied between 14 and 15.4 dB, with a power-added-efficiency of over 30%. Common Titanium Oxide substrates were used for the input and output circuits of the two MMICs, continued on both sides by Lange couplers on Alumina substrates. The entire module resulted 7.5 mm x 8.9 mm in size. Its layout can be seen in Fig. 6.

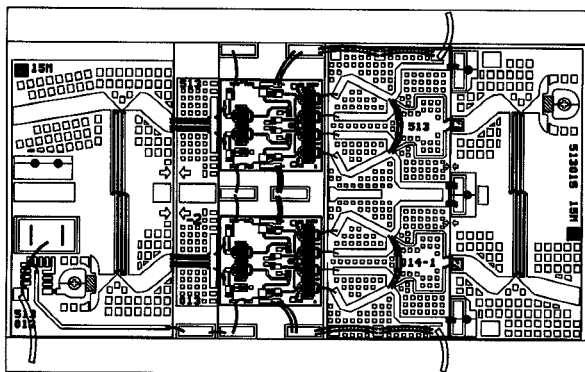


Fig. 6: Layout of the 6W 8.5-10.5 GHz balanced module

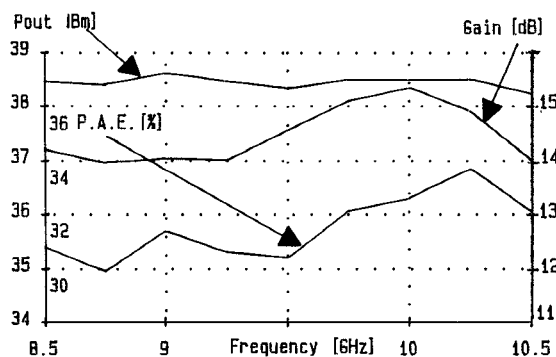


Fig. 7: Performance of the 6W module from Fig. 6.

Finally, a higher power module featured a balanced structure using Lange couplers, with two of the previously described MMICs paralleled in each branch. The drain voltage was specified at +9 V. The module was required to operate between 8 and 11 GHz. Each group of two parallel MMICs operated with a single input and a single output

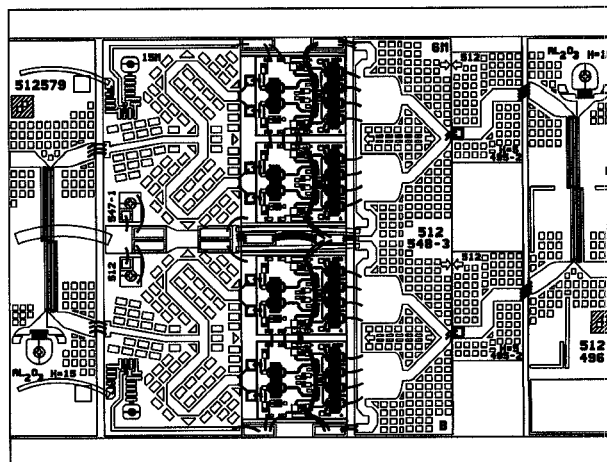


Fig. 8: Layout of the 10 W balanced module

circuit, which cumulated the functions of impedance matching and of power dividing/combining. Fig. 9 indicates that the output power was higher than 39 dBm (at 2 dB gain compression), the power-added-efficiency exceeded 23% and the associated gain varied within the range of 10 to 14 dB. The parameters are noticeably better for frequencies up to 10.5 GHz and the plots suggest that the range within which full performance is achieved extends well below the specified limit of 8 GHz. The carrier that supports the module has an area of 12 mm x 11 mm and is shown in Fig. 8.

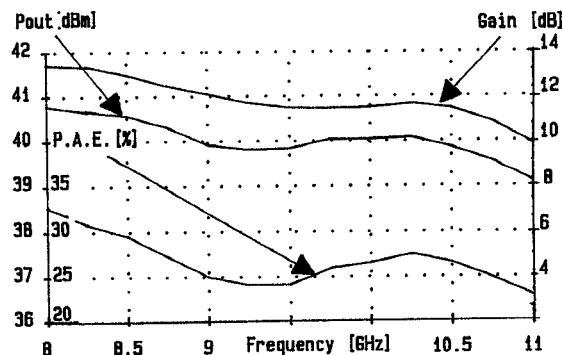


Fig. 9: Performance of the 10W module from Fig. 8

### Conclusions.

Development of a new high power and high efficiency amplifying MMIC was based on considerations of compatibility with a broad range of X-band applications, which differ in frequency range, bias conditions and special requirements. It operates as a building block for use in power modules, in conjunction with external matching circuits on separate ceramic substrates. The modules can be easily reconfigured for specific applications by redesigning the input and output hybrid circuits only, at low cost and in a time frame that would not allow the development of new MMICs. The MMIC was utilized so far as the active device in four different types of power modules and superior performance could be obtained in each case. The chip size was reduced to a minimum by including in it only the most critical elements, while the overall size of the modules remained competitive with fully monolithic implementations.

### Acknowledgments.

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### References.

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2. "A 1.6-Watt High Efficiency X-Band Power MMIC", M. Avasarala et al., 1989 IEEE GaAs IC Symposium Technical Digest, pp. 263-266.